1. A method to fabricate silicon nitride sidewall spacers in the manufacture of an integrated circuit device comprising:

providing an insulating layer overlying a semiconductor substrate;

providing polysilicon traces overlying said insulating layer;

forming a liner oxide layer overlying said polysilicon traces and said insulating layer;

forming a silicon nitride layer overlying said liner oxide layer;

depositing a silicon layer overlying said silicon nitride layer;

oxidizing completely said silicon layer to form a temporary silicon dioxide layer wherein the corners of said temporary silicon dioxide layer are rounded due to volume expansion during said oxidizing step;

anisotropically etching said temporary silicon dioxide layer to expose horizontal surfaces of said silicon nitride layer while leaving vertical surfaces of said temporary silicon dioxide layer remaining; and

thereafter anisotropically etching said exposed silicon nitride layer to form said silicon nitride sidewall spacers in the manufacture of the integrated circuit

device.

2. The method according to Claim 1 wherein said polysilicon traces comprise transistor gates.

3. The method according to Claim 1 wherein said liner oxide layer is formed to a thickness of between about 50 Angstroms and 300 Angstroms.

4. The method according to Claim 1 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

5. The method according to Claim 1 wherein said silicon nitride layer is formed to a thickness of between about 100 Angstroms and 700 Angstroms.

6. The method according to Claim 1 wherein said silicon layer is deposited to a thickness of between about 50 Angstroms and 400 Angstroms.

7. The method according to Claim 1 wherein said silicon layer comprises one of the group of: polysilicon and amorphous silicon.

8. The method according to Claim 1 wherein said step of oxidizing completely is by a low temperature oxidation process with an oxidation temperature of between about 650 degrees C and 800 degrees C, additive gases comprising chlorine containing gases, and ambient gases comprising one of the group of: O_2 with H_2 and O_2 with N_2.

9. The method according to Claim 1 wherein said silicon nitride sidewall spacers have an L-shaped profile.

10. A method to fabricate transistors with silicon nitride sidewall spacers in the manufacture of an integrated circuit device comprising:

providing a semiconductor substrate;

providing polysilicon transistor gates overlying said semiconductor substrate wherein said polysilicon transistor gates comprise: a thin gate oxide layer overlying said semiconductor substrate, a polysilicon gate electrode overlying said thin gate oxide layer, and lightly doped drains formed in said semiconductor substrate;

forming a liner oxide layer overlying said polysilicon gates and said semiconductor substrate;

forming a silicon nitride layer overlying said liner oxide layer;

depositing a silicon layer overlying said silicon nitride layer wherein said silicon layer comprises one of the group of: polysilicon and amorphous silicon;

oxidizing completely said silicon layer to form a temporary silicon dioxide layer wherein the corners of said temporary silicon dioxide layer are rounded due to volume expansion during the oxidation step;

anisotropically etching said temporary silicon dioxide layer to expose horizontal surfaces of said silicon nitride layer while leaving vertical surfaces of said temporary silicon dioxide layer remaining;

anisotropically etching said exposed silicon nitride layer to form L-shaped silicon nitride sidewall spacers; and

depositing an interlevel dielectric layer overlying said polysilicon transistor gates and said silicon nitride sidewall spacers to complete transistors in the manufacture of said integrated circuit device.

11. The method according to Claim 10 wherein said liner oxide layer is formed to a thickness of between about 50 Angstroms and 300 Angstroms.

12. The method according to Claim 10 wherein said silicon nitride layer is formed by one of the group of: growing by thermal process and depositing by chemical vapor deposition.

13. The method according to Claim 10 wherein said silicon nitride layer is formed to a thickness of between about 100 Angstroms and 700 Angstroms.

14. The method according to Claim 10 wherein said silicon layer is deposited to a thickness of between about 50 Angstroms and 400 Angstroms.

15. The method according to Claim 10 wherein said step of oxidizing completely is by a low temperature oxidation process with an oxidation temperature of between about 650 degrees C and 800 degrees C, additive gases comprising chlorine containing gases, and ambient gases comprising one of the group of: O_2 with H_2 and O_2 with N_2.

16. The method according to Claim 10 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon dioxide, silicon nitride, and silicon oxynitride.

17. A MOSFET device comprising:

an insulator layer overlying a semiconductor substrate;

polysilicon traces overlying said insulator layer;

a liner oxide layer overlying said polysilicon traces;

silicon nitride spacers on sidewalls of said polysilicon traces and overlying said liner oxide layer wherein said silicon nitride spacers have an L-shaped profile; and

an interlevel dielectric layer overlying said polysilicon traces, said silicon nitride spacers, and said liner oxide layer.

18. The device according to Claim 17 wherein said liner oxide layer has a thickness of between about 50 Angstroms and 300 Angstroms.

19. The device according to Claim 17 wherein said polysilicon traces comprise transistor gates.

20. The device according to Claim 17 wherein said interlevel dielectric layer comprises a combination material from the group of: TEOS undoped oxide, boron phosphosilicate glass (BPSG), undoped silicon dioxide, silicon nitride, and silicon oxynitride.